

FIG. 1

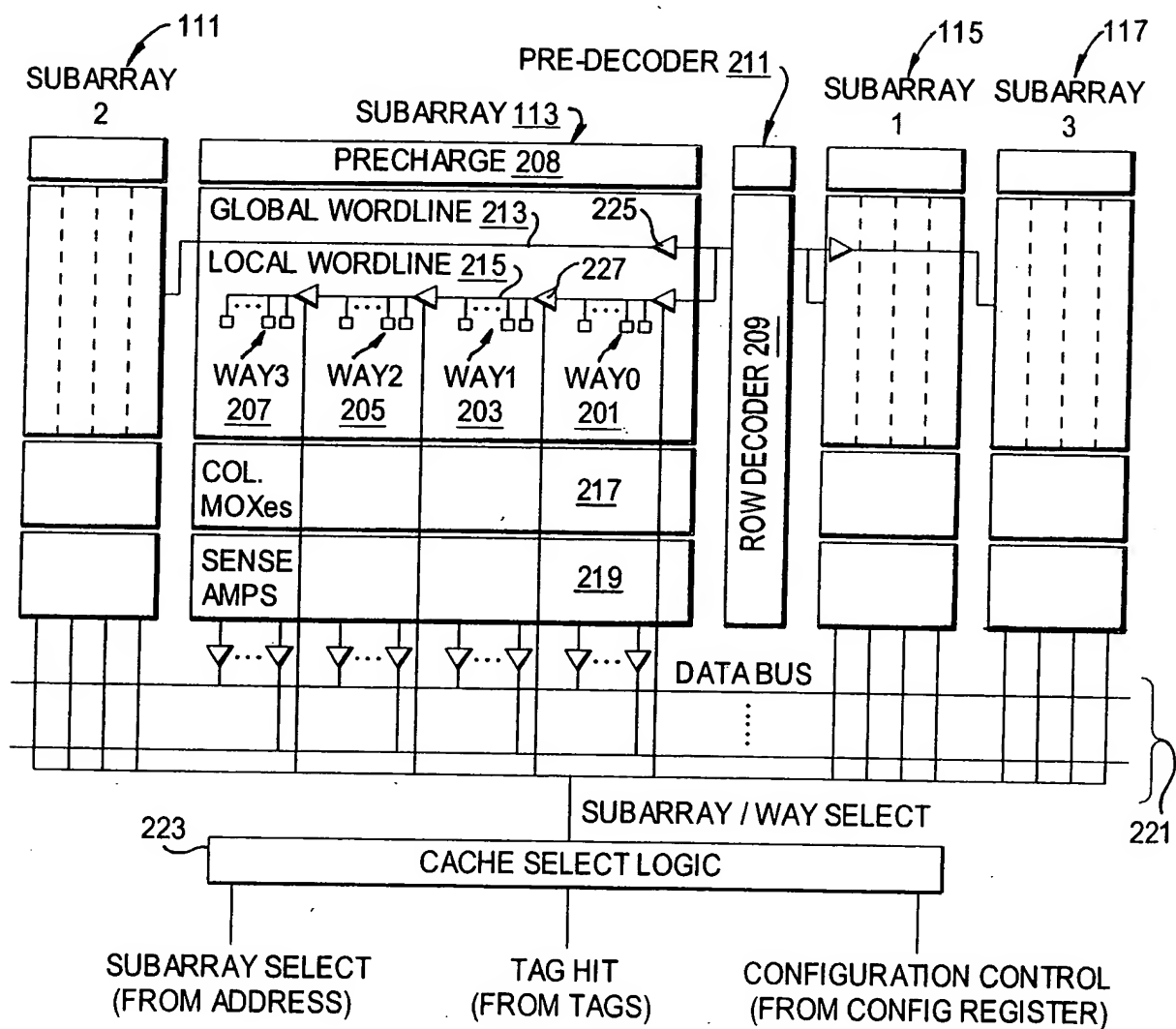


FIG. 2

SUBARRAY / WAY ALLOCATION (L1 OR L2)

CACHE CONFIGURATION	L1 SIZE	L1 ASSOC	L1 ACC TIME	SUBARRAY 2												SUBARRAY 0				SUBARRAY 1				SUBARRAY 3			
				SUBARRAY 2				SUBARRAY 0				SUBARRAY 1				SUBARRAY 3				SUBARRAY 1				SUBARRAY 3			
				W3	W2	W1	W0	W3	W2	W1	W0	W3	W2	W1	W0	W3	W2	W1	W0	W3	W2	W1	W0	W3	W2	W1	W0
256-1	256KB	1 WAY	2.0	L2	L2	L2	L2	L2	L2	L2	L1	L1	L2	L2	L1	L1	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2
512-2	512KB	2 WAY	2.5	L2	L2	L2	L2	L2	L2	L2	L1	L1	L2	L2	L1	L1	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2
768-3	768KB	3 WAY	2.5	L2	L2	L2	L2	L2	L2	L2	L1	L1	L2	L2	L1	L1	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2
1024-4	1024KB	4 WAY	3.0	L2	L2	L2	L2	L2	L2	L2	L1	L1	L2	L2	L1	L1	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2
512-1	512KB	1 WAY	3.0	L2	L2	L2	L2	L2	L2	L2	L1	L1	L2	L2	L1	L1	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2
1024-2	1024KB	2 WAY	3.5	L2	L2	L2	L2	L2	L2	L2	L1	L1	L2	L2	L1	L1	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2	L2
1536-3	1536KB	3 WAY	4.0	L2	L1	L1	L1	L2	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L2	L1	L1	L1	L1	L1	L1	L2
2048-4	2048KB	4 WAY	4.5	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1

FIG. 3

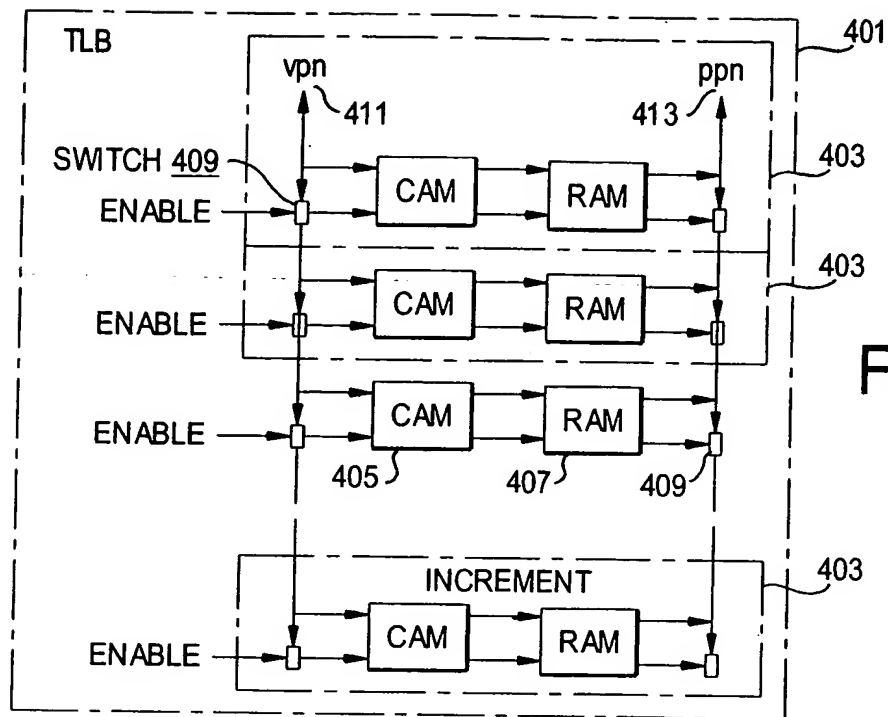
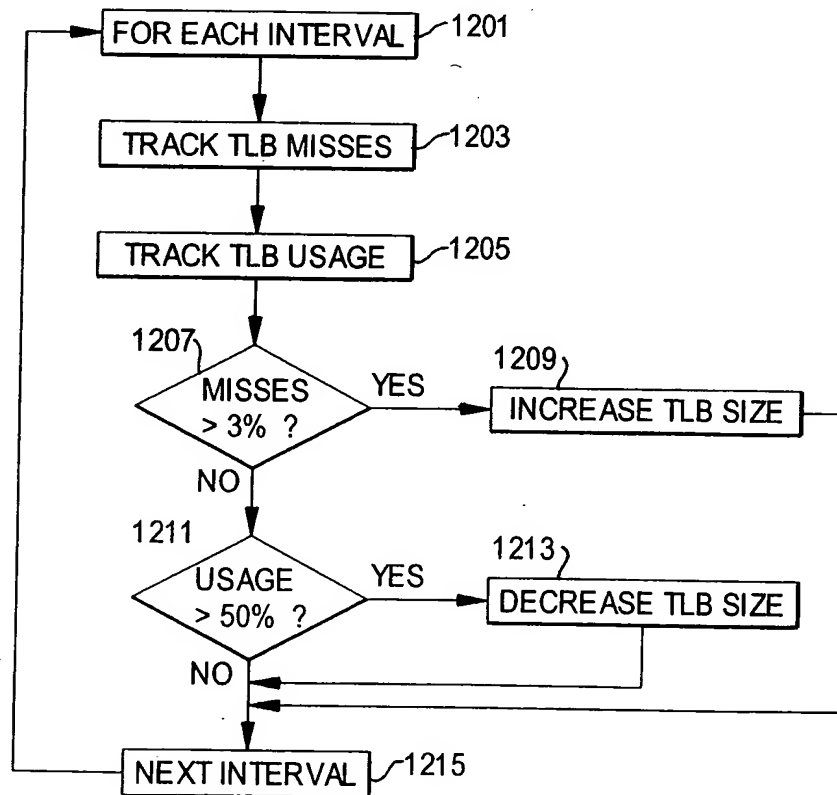


FIG. 4

FIG. 12



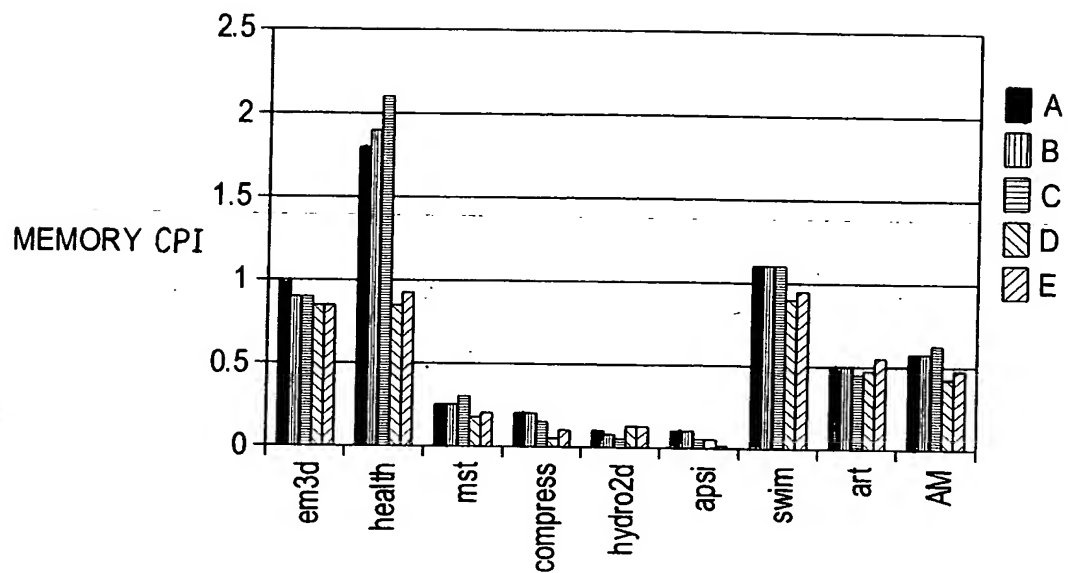


FIG. 5

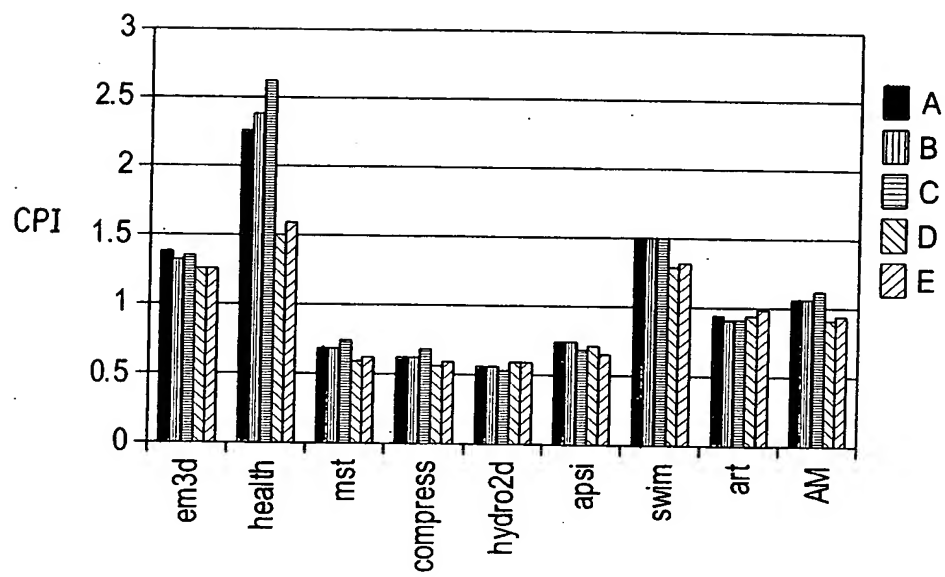


FIG. 6

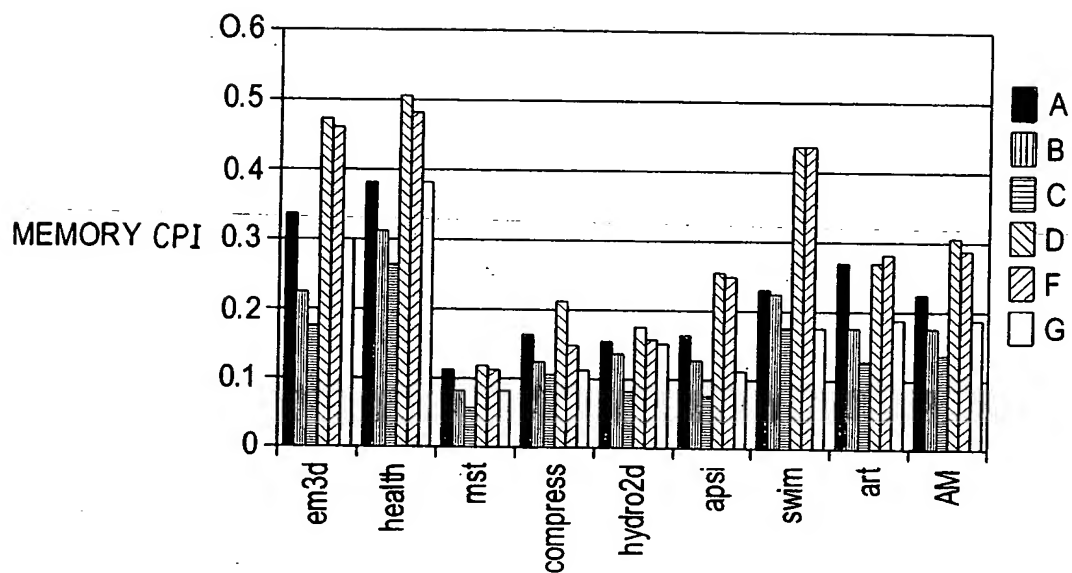


FIG. 7

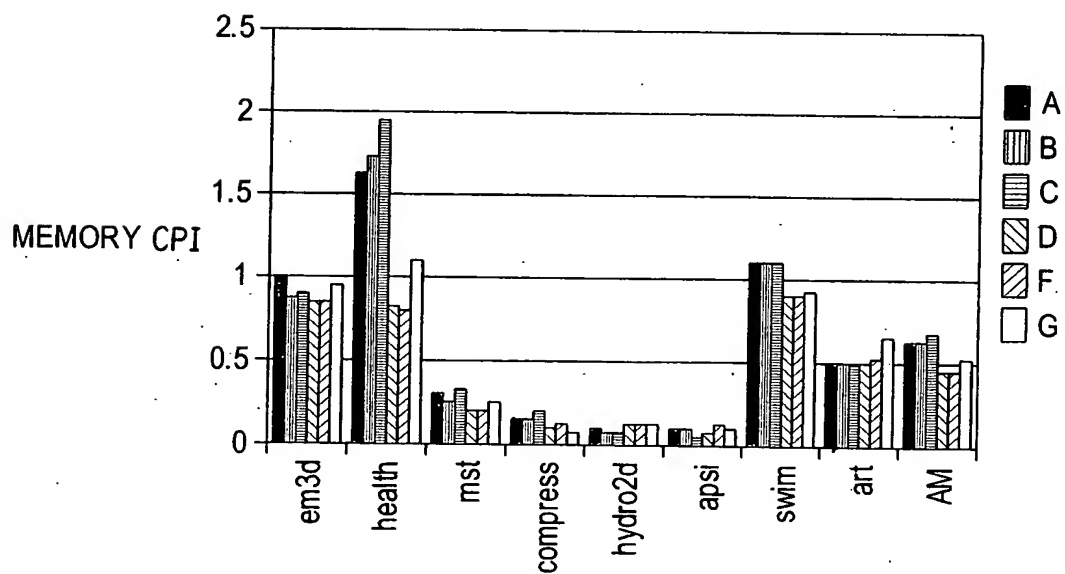


FIG. 8

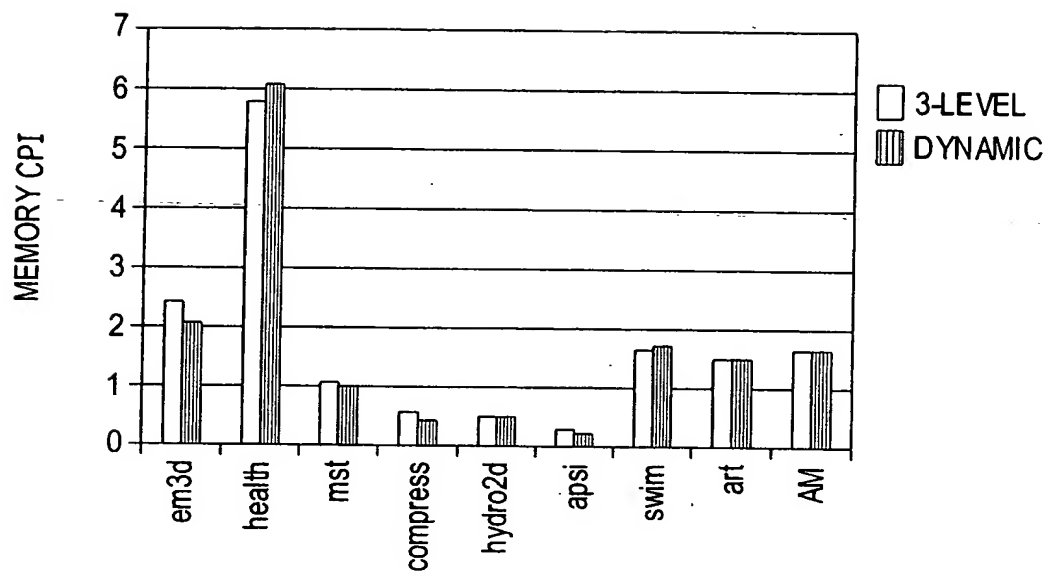


FIG. 9

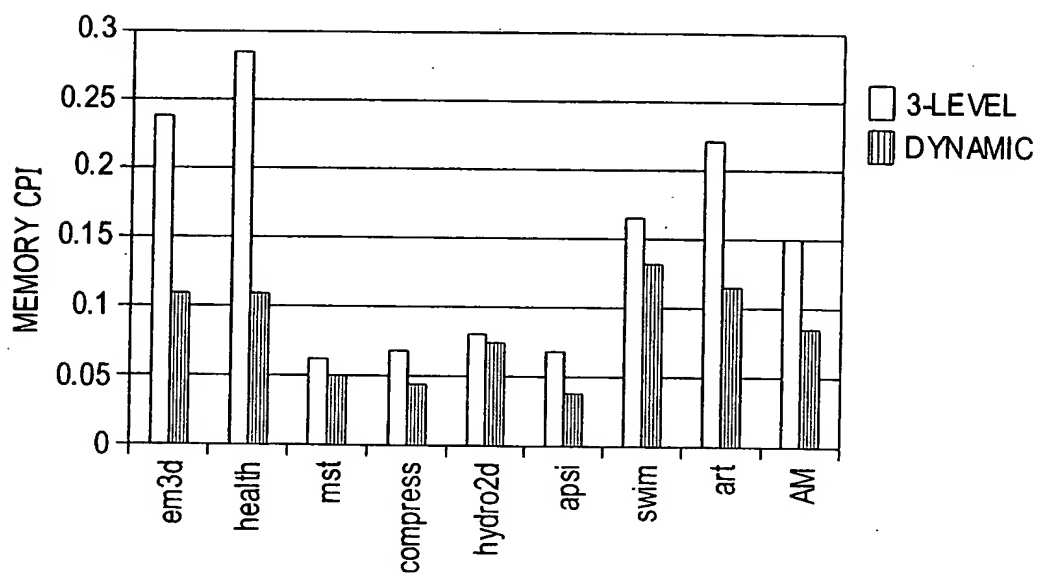


FIG. 10

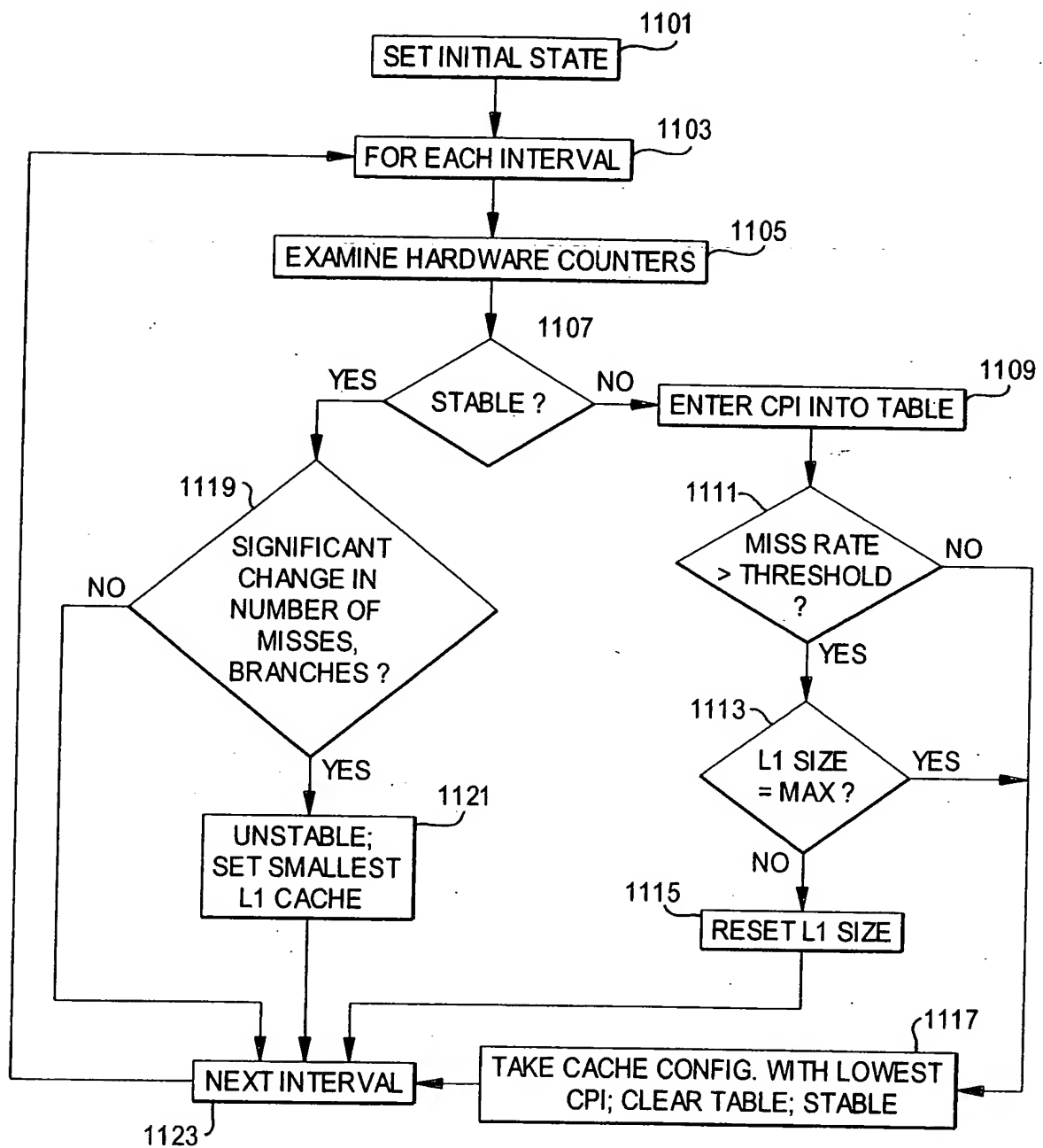


FIG. 11